PXIe-9702

Arbitary Waveform Generator Modules

User Manual

User Manual Version: 1.0.7

Revision Date: September 9, 2024

Table of Contents

1.Introduction 1
1.1 Overview 1
1.2 Main Features 1
1.3 Abbreviations 1
1.4 Learn by Examples 1
2.Hardware Specifications 4
2.1 Analog Output Specifications 4
2.2 Analog Output Accuracy 4
2.3 PFI Specifications 5
2.4 Trigger In 5
2.5 Frequency and Transient Response 5
2.6 DDS Mode Maximum Frequencies 5
2.7 Timing Specifications 6
2.8 Front Panel and Pin Definition 7
3.Performance and Tests 9
3.1 Average Noise Density 9
3.2 Spurious-Free Dynamic Range (SFDR) 9
3.3 -3db Bandwith 10
3.4 Total Harmonic Distortion 10
4.Software 12
4.1 System Requirements 12
4.2 System Software 13
4.3 C# Programming Language 13
4.4 PXIe-9702 Series Hardware Driver 13
4.5 Install the SeeSharpTools from JYTEK 14
4.6 Running C# Programs in Linux 14
5.Operating PXIe-9702 15
5.1 Quick Start 15
5.2 Trigger Source 15
5.2.1 Immediate trigger 16
5.2.2 Software Trigger 18
5.2.3 External Digital Trigger 20
5.3 Trigger Mode 23
5.3.1 Start Trigger 23
5.4 AO Operations 23
5.4.1 Finite Output 23
5.4.2 Continuous NoWrappping Output 26
5.4.3 Continuous Wrapping Output 29
5.4.4 DDS 32
5.4.5 Output Wave From File 33

6.Calibration **35**
7.Using PXIe-9702 in Other Software **36**
7.1 Python 36
7.2 C++ 36
7.3 LabVIEW 36
8.About JYTEK **37**
8.1 JYTEK China 37
8.2 JYTEK Software Platform 37
8.3 JYTEK Warranty and Support Services 37
9.Statement **38**

Table 1 Analog Output Specifications 4
Table 2 Analog Output Accuracy 4
Table 3 PFI Specifications 5
Table 4 Trigger In Specifications 5
Table 5 Frequency and Transient Response 5
Table 6 Suggested Maximum Frequencies 5
Table 7 Timing Specifications 6
Table 8 PXIe-9702 Pin Definition 8
Table 9 Average Noise Density 9
Table 10 Spurious-Free Dynamic Range (SFDR) 9
Table 11 Total Harmonic Distortion, Direct Path, Typical 10
Table 12 Total Harmonic Distortion, Low-Gain Amplifier Path, Typical 11
Table 13 Total Harmonic Distortion, Low-Gain Amplifier Path, Typical 11
Table 14 Supported Linux Versions 12
Table 15 Non-Configurable Update Rate Intervals 15

Figure 1 JYPEDIA Information 2
Figure 2 Connect the oscilloscope's CH1 to PXIe-9702's CH0 2
Figure 3 Connect the oscilloscope's CH1 and CH2 to PXIe-9702's CH0 and CH1 3
Figure 4 PXIe-9702 Front Panel 7
Figure 5 PXIe-9702 Connector Side View 8
Figure 6 3 -3db Bandwith 10
Figure 7 Total Harmonic Distortion, Direct Path, Typical 10
Figure 8 Total Harmonic Distortion, High-Gain Amplifier Path, Typical 11
Figure 9 Total Harmonic Distortion, High-Gain Amplifier Path, Typical 12
Figure 10 Immediate trigger Paraments 17
Figure 11 Generated Signal 18
Figure 12 Scope Acquisition AO Signal 18
Figure 13 Software Trigger Paraments 19
Figure 14 Software Trigger Acquisition 19

Figure 15 Scope Acquisition AO Signal....20
Figure 16 External Digital Trigger....20
Figure 17 Digital Trigger Paraments....21
Figure 18 Digital Trigger Acquisition....22
Figure 19 Scope Acquisition AO Signal....22
Figure 20 Start Trigger....23
Figure 21 AO Finite Output Paraments....24
Figure 22 AO Finite Signal....25
Figure 23 AO Finite Signal (External Clock Source)....25
Figure 24 Scope Acquisition AO signal....25
Figure 25 AO Continuous NoWrapping Output Paraments....26
Figure 26 AO Continuous NoWrapping Signal....27
Figure 27 Scope Acquisition AO signal....27
Figure 28 AO Continuous NoWrapping Signal....28
Figure 29 Scope Acquisition AO signal....28
Figure 30 AO Continuous Wrapping Paraments....29
Figure 31 AO Continuous Wrapping Signal....30
Figure 32 Scope Acquisition AO signal....30
Figure 33 AO Continuous Wrapping MultiChannel Paraments....31
Figure 34 Scope Acquisition AO signal....31
Figure 35 AO Standard Waveform generation Paraments....32
Figure 36 Scope Acquisition AO signal....33
Figure 37 Generated Signal....34
Figure 38 Received Signal....35

1. Introduction

This chapter presents the information how to use this manual and how to quick start if you are already familiar with Microsoft Visual Studio and C# programming language.

1.1 Overview

PXIe-9702 arbitrary waveform generator modules provide 2-channel, 16 bits DAC, up to 250 MS/s update rate per channel. which can run in PXIe system.

1.2 Main Features

- Max 250MS/s Update Rate
- 2 analog output channels
- 16 bits DAC
- 3 output voltage ranges: ±0.5V/±1.25V/±5V with a 50 Ω load, ±1 V/±2.5 V/±10 V with a 100 kΩ load
- 512 MB DDR3 memory
- PCIe GEN2x4 high speed interface
- ports of bidirectional 3.3V LVTTL digital IO
- One external digital trigger
- One external sync clock connect
- DMA for analog output
- Digital/Software Trigger
- Windows and Linux Support

1.3 Abbreviations

AO: Analog Output
DAC: Digital-to-Analog Conversion

1.4 Learn by Examples

JYTEK has added Learn by Example in this manual. We provide many sample programs for this device. Please download the sample programs for this device. You can download a JYPEDIA excel file from our web www.jytek.com. Open JYPEDIA and search for PXIe-9702 in the driver sheet, select JYPXIe-9702 Examples.zip. In addition to the download information, JYPEDIA also has a lot of other valuable information, JYTEK highly recommend you use this file to obtain information from JYTEK.

Drivers	Update Date	Category
JYPXIe-9702_V1.0.1_Examples.zip	2022/3/18	Example
JYPXIe-9702_V1.0.1_Win.zip	2021/11/12	Driver
JYPXIe-9702_V1.0.0_Linux.tar	2021/11/12	Driver

Figure 1 JYPEDIA Information

In a Learn by Example section, the sample program is in bold style such as **Analog Output-->Winform AO Continuous NoWrapping**; the property name in the sample program is also in bold style such as **Trigger source**; the technical names used in the manual is in italic style such as Software trigger. You can easily relate the property names in the example program with the manual documentation.

In an Learn by Example section, the experiment is set up as follow. A PXIe-9702 card is connected to an oscilloscope. Connect the oscilloscope's CH1 to PXIe-9702's CH0 as shown in Figure 2. Connect the oscilloscope's CH1 and CH2 to PXIe-9702's CH0 and CH1 as shown in Figure 3.

Figure 2 Connect the oscilloscope's CH1 to PXIe-9702's CH0

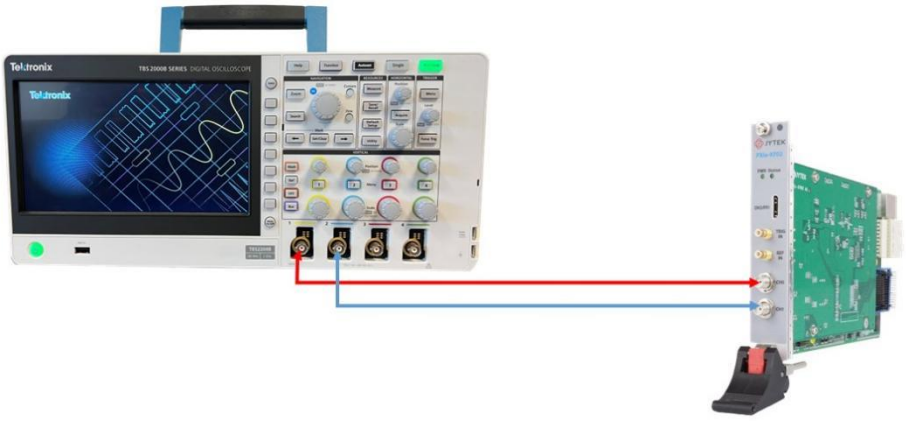

Figure 3 Connect the oscilloscope’s CH1 and CH2 to PXIe-9702’s CH0 and CH1

2. Hardware Specifications

2.1 Analog Output Specifications

Channel Number	2
Output Impedance	50 Ω
DAC Resolution	16 bits
Coupling	DC
Amplitude Range(50 Ω load)	±0.5 V
	±1.25 V
	±5 V
Amplitude Range(100 kΩ load)	±1 V
	±2.5 V
	±10 V
DC gain error	±0.05%
DC offset error	±0.08% of Amplitude Range
Connector type	SMA

Table 1 Analog Output Specifications

2.2 Analog Output Accuracy

JY-9702 Basic Accuracy = ±(% Reading+% Range)											
Nominal Range (V)	24 Hour Tcal ±1°C			90 Days Tcal±5°C			Temperature Coefficients(/°C)			24 Hr Full Scale Accuracy	90 Days Full Scale Accuracy
1	0.14	+	0.05	0.36	+	0.07	0.007	+	0.005	2 mV	5 mV
2.5	0.13	+	0.05	0.34	+	0.07	0.007	+	0.007	5 mV	11 mV
10	0.12	+	0.06	0.32	+	0.08	0.013	+	0.006	17 mV	39 mV
Accuracy valid to 95% of full range											

Table 2 Analog Output Accuracy

2.3 PFI Specifications

Connector type	Mini HDMI
Channnel number	8
Destinations	Bidirectional
Frequency range	30 MHz
Voltage	3.3 V LVCMOS
Impedance	50 Ω
Coupling	DC

Table 3 PFI Specifications

2.4 Trigger In

Connector type	SMB
Channnel number	1
Destinations	Bidirectional
Frequency range	30 MHz
Voltage	3.3 V LVCMOS
Impedance	50 Ω
Coupling	DC

Table 4 Trigger In Specifications

2.5 Frequency and Transient Response

Analog filter	Passband: 100 MHz@ 1.1 dB Stopband: 450 MHz@-80 dB
Passband Flatness	1.1 dB

Table 5 Frequency and Transient Response

2.6 DDS Mode Maximum Frequencies

Sine	±1 V(100 MHz), ±2.5 V(80 MHz) ,±10 V(50 MHz至60 MHz)
Square	±1 V/ ±2.5 V/±10 V(10MHz)
Triangle	±1 V/ ±2.5 V/±10 V(20MHz)

Table 6 Suggested Maximum Frequencies

2.7 Timing Specifications

Sample Clock		
Source	Internal:	PLL-based
Sample Rate Range	31.25 MHz ~ 250 MHz	
Onboard Clock (Internal TCXO)		
Frequency accuracy	2 ppm	
Phase-Locked Loop (PLL) Reference Clock		
Sources	PXIe_CLK100 CLK IN Internal TCXO	
Frequency accuracy	Dependent on the frequency accuracy of the PLL Reference Clock source	
Lock time	≤1000 ms,	
Duty cycle range	40% to 60%	
CLock IN		
Connector type	SMB	
Destinations	PLL Reference Clock	
Frequency range	10MHz	
Input voltage range into 50 Ω	Sine wave:	0.5 V pk-pk to 2.4 V pk-pk
	Square wave:	0.5 V pk-pk to 2.4 V pk-pk
Maximum input overload	±3.3 V	
Impedance	50 Ω	
Coupling	AC	

Table 7 Timing Specifications

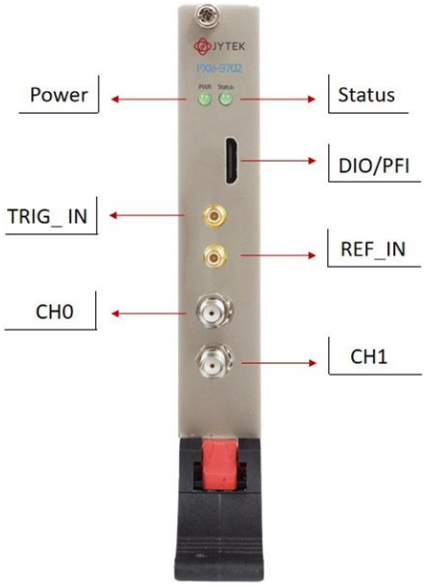

Figure 4 PXIe-9702 Front Panel

2.8 Front Panel and Pin Definition

9702 seires boards has 2 SMA connectors for output signals: CH0 and CH1 as shown in Table 8. Trigger and Reference clock signals connect to 9702 via TRIG_in and REF_IN SMB connectors as shown in Table 8, DIO/PFI function can be used with miniHDMI connector. Mini-HDMI pin definition and pin definition after HDMI adapting are shown in following Table 8

9702 Connector Pin Definition

PXIe-9702 Connector Pin Definition		
pin number	Mini-HDMI pin definition	After HDMI adapting
1	GND	PFI0
2	PFI0	GND
3	PFI1	PFI1
4	GND	PFI2
5	PFI2	GND
6	PFI3	PFI3
7	GND	PFI4
8	PFI4	GND
9	PFI5	PFI5
10	GND	PFI6
11	PFI6	GND
12	PFI7	PFI7
13	GND	GND
14	NC	NC
15	NC	NC
16	NC	NC
17	NC	NC
18	3.3V OUT 300mA Limited output impendance <1Ω	3.3V OUT 300mA Limited output impendance <1Ω
19	NC	NC

Table 8 PXIe-9702 Pin Definition

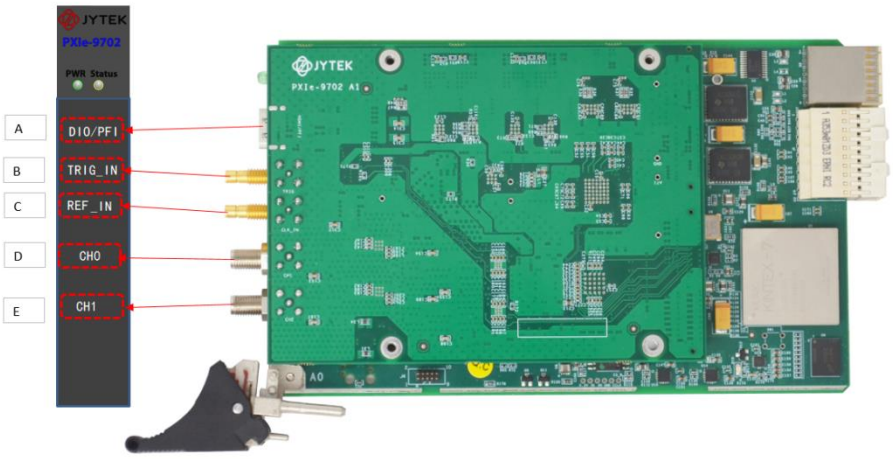

Figure 5 PXIe-9702 Connector Side View

3. Performance and Tests

3.1 Average Noise Density

CH0 Noise,Output Signal 45MHz，40M Filter						
Voltage Range	Normalized Amplitude	No Filter Signal	After Filter Signal	Filter Insertion Loss	dBm/Hz	dBFS/Hz
±0.5 V(50 Ω load)	0.95	3.08	0.68	-2.4	150.02	150.7
±1.25 V(50 Ω load)	0.95	11.45	8.87	-2.58	142.11	150.98
±5 V(50 Ω load)	0.95	23.59	19.93	-3.66	130.46	150.39

CH1 NoiseOutput Signal 45MHz，40M Filter						
Voltage Range	Normalized Amplitude	No Filter Signal	After Filter Signal	Filter Insertion Loss	dBm/Hz	dBFS/Hz
±0.5 V(50 Ω load)	0.95	3.08	0.68	-2.4	150	150.68
±1.25 V(50 Ω load)	0.95	11.45	8.87	-2.58	142	150.87
±5 V(50 Ω load)	0.95	23.59	19.93	-3.66	130	149.93

Table 9 Average Noise Density

3.2 Spurious-Free Dynamic Range (SFDR)

Frequency	Direct path		Low-Gain Amplifier Path		High-Gain Amplifier Path	
	CH1	CH2	CH1	CH2	CH1	CH2
1.00	71.10	71.26	65.14	65.34	73.06	72.84
5.00	72.38	72.37	64.00	64.05	69.91	69.00
10.00	72.10	71.19	60.94	60.82	65.24	65.07
20.00	70.81	68.63	57.36	57.12	60.43	60.08
30.00	69.44	66.30	54.56	54.17	56.60	56.09
40.00	66.77	63.59	51.80	51.46	53.13	52.66
50.00	65.70	62.33	49.73	49.15	50.10	49.52
60.00	66.16	62.28	47.90	47.29	47.61	46.93
70.00	64.42	62.83	45.87	45.36	45.42	44.71
80.00	56.90	57.61	43.78	43.36	43.35	45.17
90.00	54.46	55.45	41.84	41.42	-	-
100.00	52.07	53.44	-	-	-	-

Table 10 Spurious-Free Dynamic Range (SFDR)

3.3 -3db Bandwith

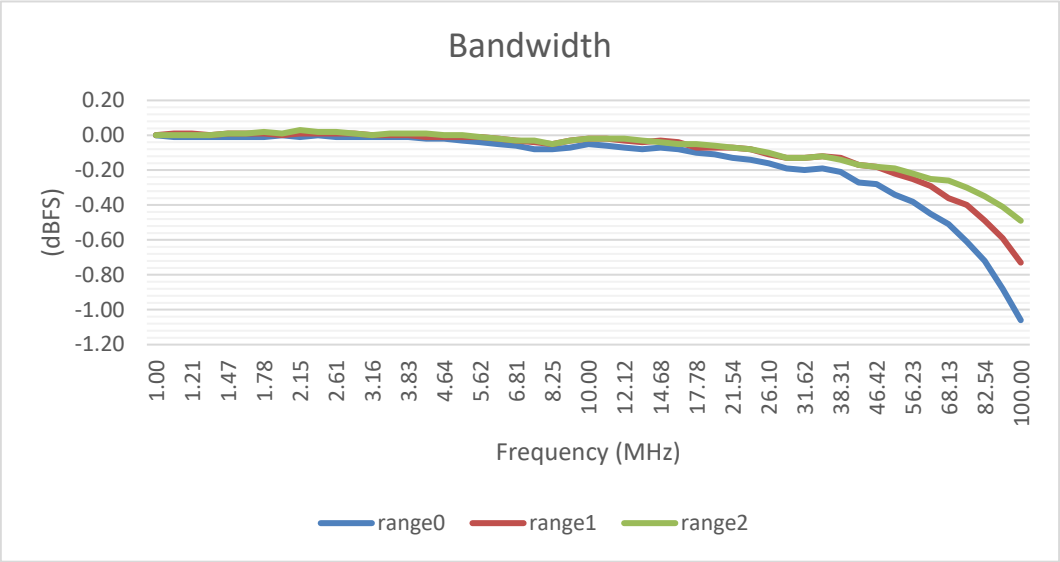

Figure 6 -3db Bandwith

3.4 Total Harmonic Distortion

Frequency	1	5	10	20	30	40	50	60	70	80	90	100
CH1	-70.00	-71.90	-71.47	-70.16	-68.66	-65.77	-63.00	-61.44	-58.36	-55.81	-53.41	-50.26
CH2	-70.13	-71.70	-70.49	-67.92	-65.68	-62.91	-60.94	-59.70	-58.26	-56.58	-55.06	-52.10

Table 11 Total Harmonic Distortion, Direct Path, Typical

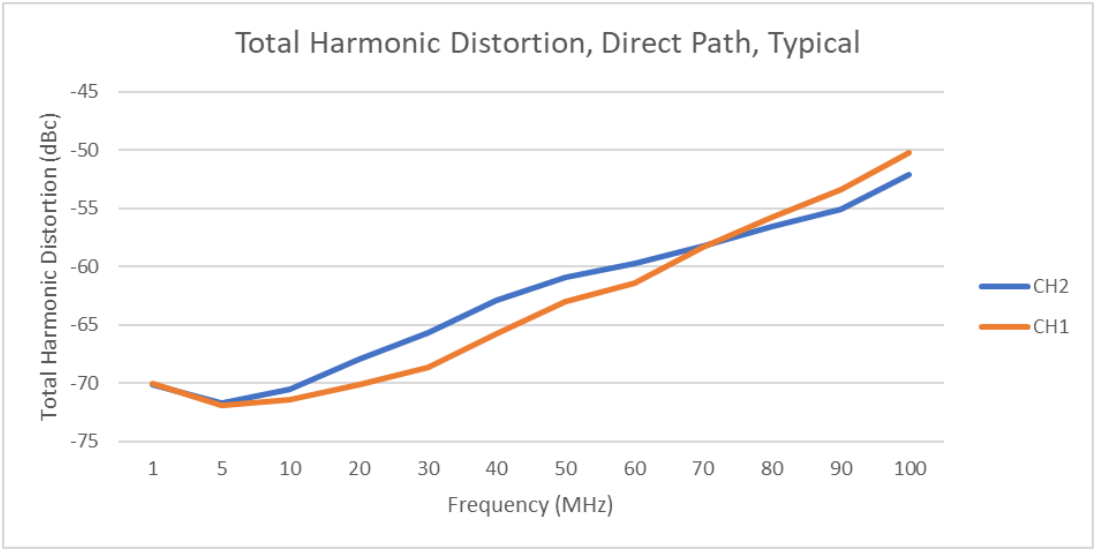

Figure 7 Total Harmonic Distortion, Direct Path, Typical

Frequency	1	5	10	20	30	40	50	60	70	80	90
CH1	-63.16	-63.75	-60.55	-57.08	-54.18	-51.09	-48.50	-46.43	-44.22	-41.91	-39.49
CH2	-63.51	-63.77	-60.46	-56.86	-53.85	-50.86	-48.20	-46.01	-43.90	-41.67	-39.25

Table 12 Total Harmonic Distortion, Low-Gain Amplifier Path, Typical

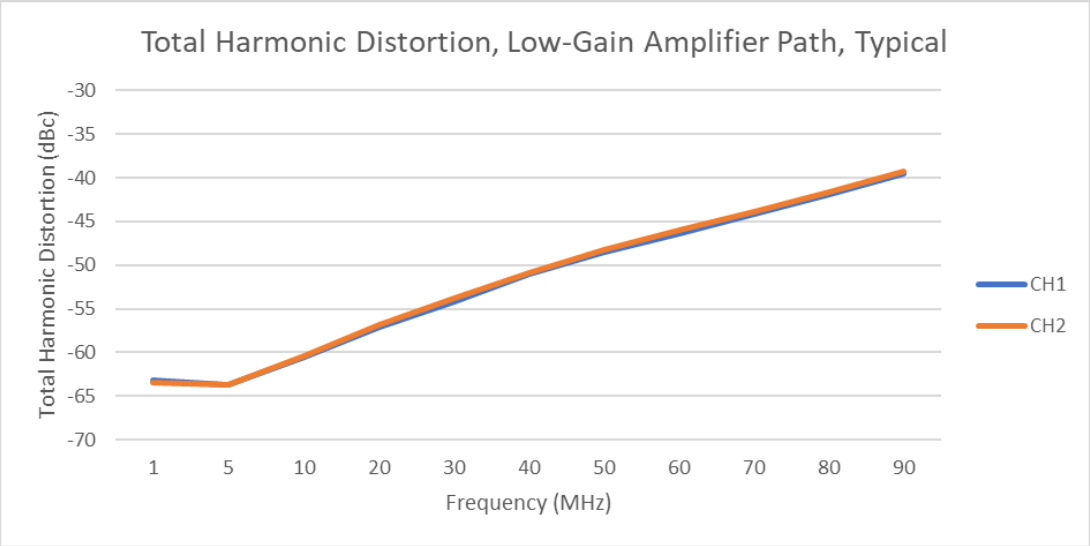

Figure 8 Total Harmonic Distortion, High-Gain Amplifier Path, Typical

Frequency	1	5	10	20	30	40	50	60	70	80
ch1	-70.68	-68.43	-63.58	-58.55	-54.73	-51.28	-48.17	-45.28	-42.24	-39.82
ch2	-70.67	-67.87	-63.7	-58.62	-54.66	-51.16	-48.18	-45.21	-42.24	-39.88

Table 13 Total Harmonic Distortion, Low-Gain Amplifier Path, Typical

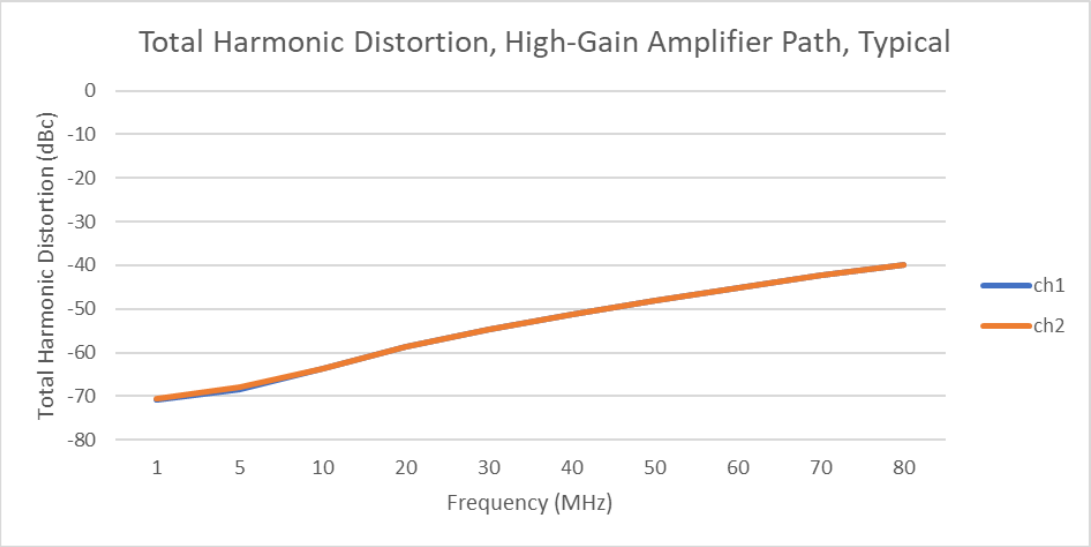

Figure 9 Total Harmonic Distortion, High-Gain Amplifier Path, Typical

4. Software

4.1 System Requirements

PXIe-9702 boards can be used in a Windows or a Linux operating system.

Microsoft Windows: Windows 7 32/64 bit, Windows 10 32/64 bit.

Linux Kernel Versions: There are many Linux versions. It is not possible JYTEK can support and test our devices under all different Linux versions. JYTEK will at the best support the following Linux versions.

Linux Version
Ubuntu LTS
16.04： 4.4.0-21-generic(desktop/server)
16.04.6：4.15.0-45-generic(desktop) 4.4.0-142-generic(server)
18.04： 4.15.0-20-generic(desktop) 4.15.0-91-generic(server)
18.04.4：5.3.0-28-generic (desktop) 4.15.0-91-generic(server)
Localized Chinese Version
中标麒麟桌面操作系统软件（兆芯版）V7.0（Build61）： 3.10.0-862.9.1.nd7.zx.18.x86_64
中标麒麟高级服务器操作系统软件V7.0U6： 3.10.0-957.el7.x86_64

Table 14 Supported Linux Versions

4.2 System Software

When using the PXIe-9702 in the Window environment, you need to install the following software from Microsoft website:

Microsoft Visual Studio Version 2015 or above,

.NET Framework version is 4.0 or above.

.NET Framework is coming with Windows 10. For Windows 7, please check .NET Framework version and upgrade to 4.0 or later version.

Given the resources limitation, JYTEK only tested PXIe-9702 be with .NET Framework 4.0 with Microsoft Visual Studio 2015. JYTEK relies on Microsoft to maintain the compatibility for the newer versions.

4.3 C# Programming Language

All JYTEK default programming language is Microsoft C#. This is Microsoft recommended programming language in Microsoft Visual Studio and is particularly suitable for the test and measurement applications. C# is also a cross platform programming language.

4.4 PXIe-9702 Series Hardware Driver

After installing the required application development environment as described above, you need to install the PXIe-9702 hardware driver.

JYTEK hardware driver has two parts: the shared common driver kernel software (FirmDrive) and the specific hardware driver.

Common Driver Kernel Software (FirmDrive): FirmDrive is the JYTEK's kernel software for all hardware products of JYTEK instruments. You need to install the FirmDrive software before using any other JYTEK hardware products. FirmDrive only needs to be installed once. After that, you can install the specific hardware driver.

Specific Hardware Driver: Each JYTEK hardware has a C# specific hardware driver. This driver provides rich and easy-to-use C# interfaces for users to operate various PXIe-9702 function. JYTEK has standardized the ways which JYTEK and other vendor's DAQ

boards are used by providing a consistent user interface, using the methods, properties and enumerations in the object-oriented programming environment. Once you get yourself familiar with how one JYTEK DAQ card works, you should be able to know how to use all other DAQ hardware by using the same methods.

Note that this driver does not support cross-process, and if you are using more than one function, it is best to operate in one process.

4.5 Install the SeeSharpTools from JYTEK

To efficiently and effectively use PXIe-9702 boards, you need to install a set of free C# utilities, SeeSharpTools from JYTEK. The SeeSharpTools offers rich user interface functions you will find convenient in developing your applications. They are also needed to run the examples come with PXIe-9702 hardware. Please register and down load the latest SeeSharpTools from our website, www.jytek.com.

4.6 Running C# Programs in Linux

Most C# written programs in Windows can be run by MonoDevelop development system in a Linux environment. You would develop your C# applications in Windows using Microsoft Visual Studio. Once it is done, run this application in the MonoDevelop environment. This is JYTEK recommended way to run your C# programs in a Linux environment.

If you want to use your own Linux development system other than MonoDevelop, you can do it by using our Linux driver. However, JYTEK does not have the capability to support the Linux applications. JYTEK completely relies upon Microsoft to maintain the cross-platform compatibility between Windows and Linux using MonoDevelop.

5. Operating PXIe-9702

This chapter provides the operation guides for PXIe-9702.

JYTEK provides extensive examples, on-line help and documentation to assist you to operate the PXIe-9702 board. JYTEK strongly recommends you go through these examples before writing his own application. In many cases, an example can also be a good starting point for a user application.

Special Operation Note:

The PXIe-9702 module has identified five non-configurable update rate intervals within its operational range of 31.25 MSa/s to 250 MSa/s. To avoid configuration errors, users should ensure the update rate is set outside these intervals. JYTEK software drivers include an automatic check function to validate the update rate before applying it to the hardware, generating appropriate error messages if a non-configurable rate is attempted.

Interval	Start Rate (MS/s)	Stop Rate (MS/s)
1	159.616	160.833
2	172.917	175.454
3	192.501	192.999
4	207.501	208.571
5	230.556	241.249

Table 15 Non-Configurable Update Rate Intervals

5.1 Quick Start

After you have installed the driver software and the SeeSharpTools, you are ready to use Microsoft Visual Studio C# to operate the PXIe-9702 products.

If you are already familiar with Microsoft Visual Studio C# , the quickest way to use PXIe-9702 boards is to go through our extensive examples. We provide source code of our examples. In many cases, you can modify the source code and start to write your applications.

5.2 Trigger Source

There are 3 trigger types:

- Immediate trigger
- Software trigger
- digital trigger

The trigger type is a property and set by driver software. Please find the provided software examples for more information.

5.2.1 Immediate trigger

The module will output the signal immediately after executing the AO Task without any trigger condition setting by default.

Learn by Example 5.2.1

- Connect the oscilloscope's CH1 to PXIe-9702's CH0 as shown in Figure 2.
- Open **Analog Output-->Winform AO Finite**,set the following numbers as shown.

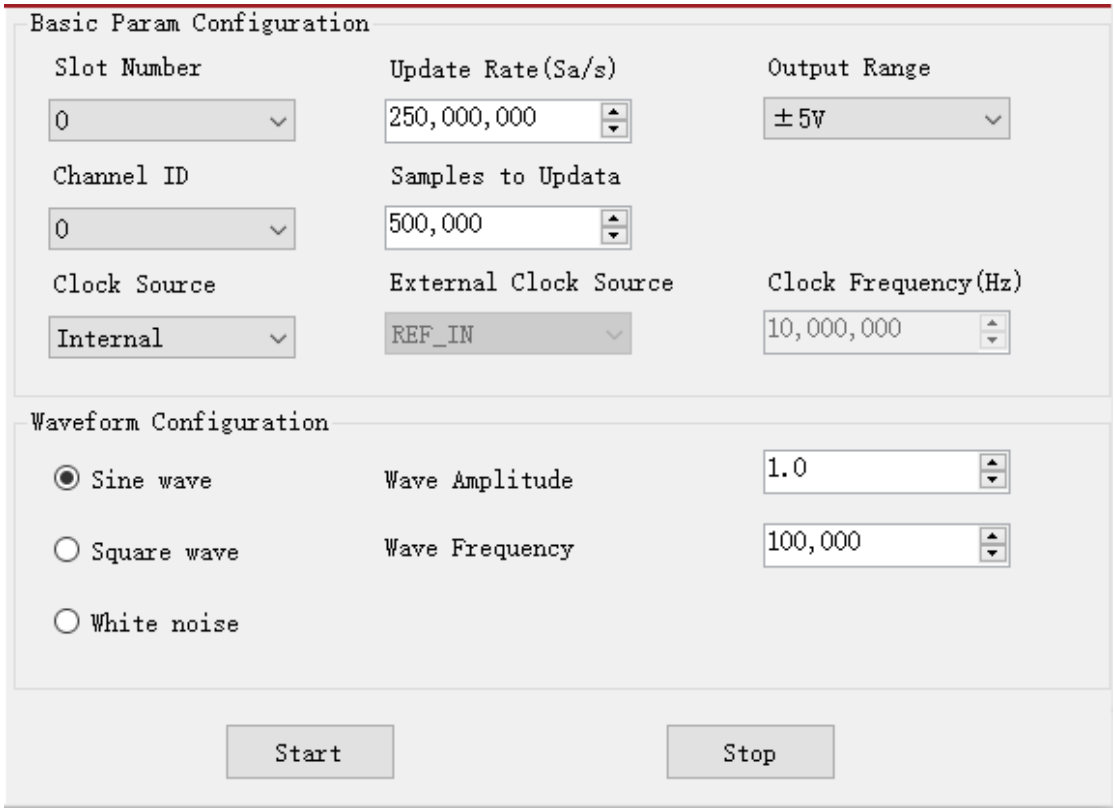

Figure 10 Immediate trigger Paraments

- With Immediate trigger you can click **Start** to generate the task insead of sending a trigger signal.

- The generated signal is shown below.

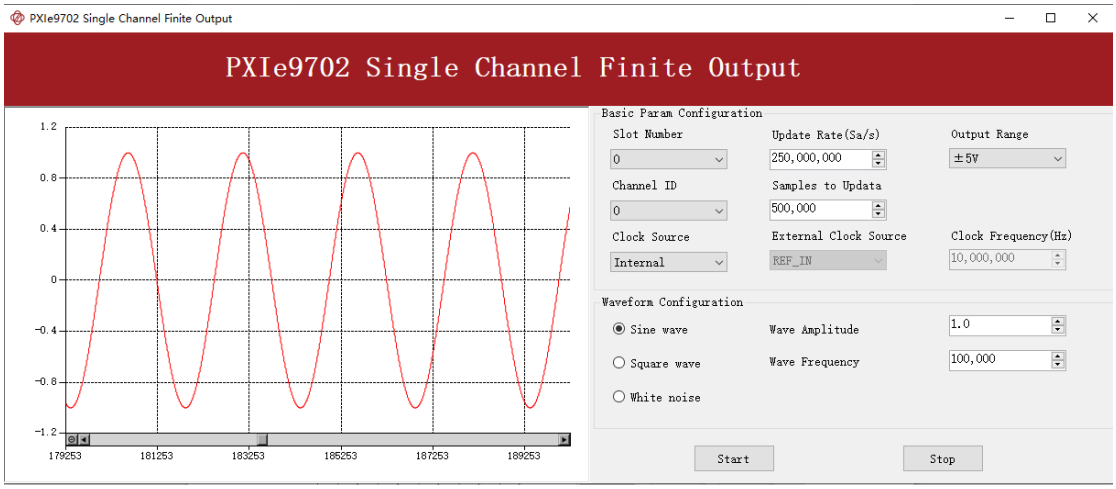

Figure 11 Generated Signal

- And the received signal is shown below.

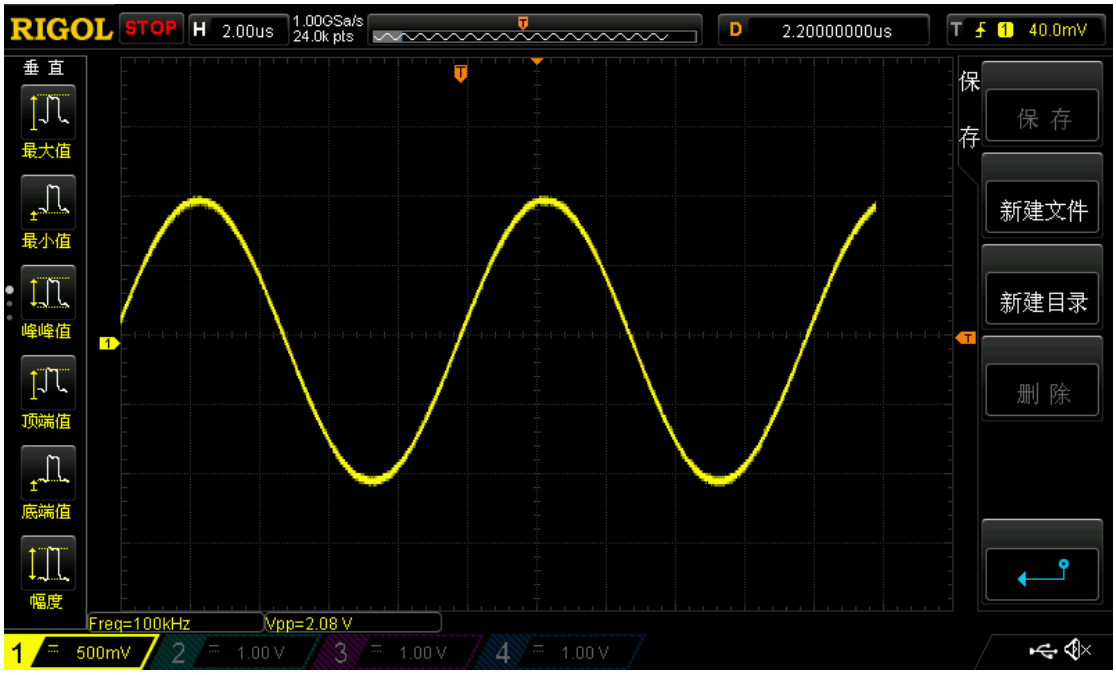

Figure 12 Scope Acquisition AO Signal

- The signal's Freq=100kHz,Vpp=2.08V,which matches the configurations set before.

5.2.2 Software Trigger

The anglog output task will wait on the software trigger signal in the software trigger mode until receiving a software trigger signal from driver, then AO task will start to acquire the data.

Learn by Example 5.2.2

- Connect the oscilloscope's CH1 to PXIe-9702's CH0 as shown in Figure 2.

■ Open **Analog Output-->Winform AO Continuous Wrapping Soft Trigger**,set the following numbers as shown.

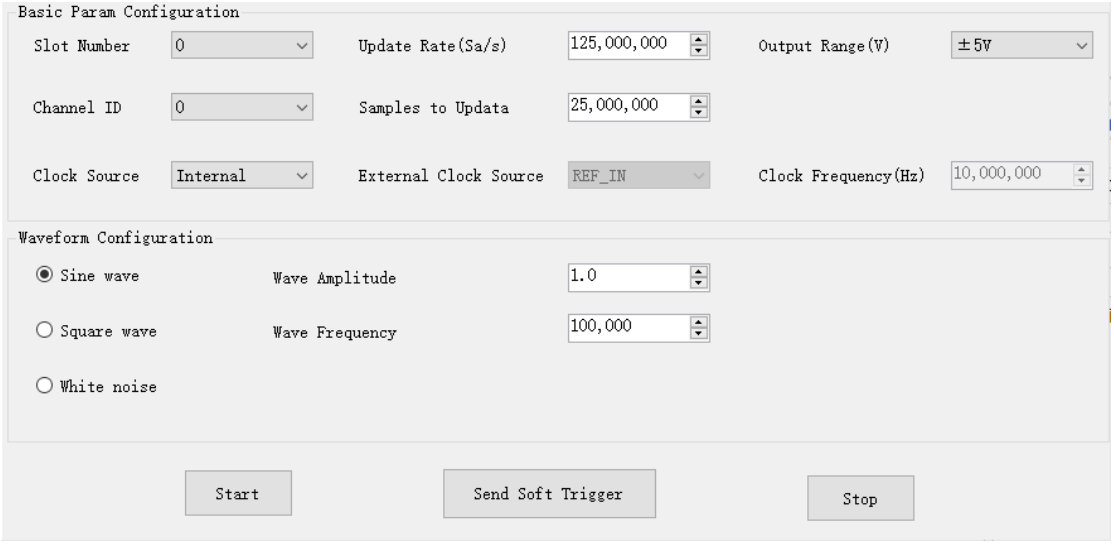

Figure 13 Software Trigger Paraments

■ Click **Start** to run the task.

➢ Signal will not be generated until there is positive signal from *Software Trigger* when Send Soft Trigger is clicked.

■ After sending the trigger signal ,the result will be like this.

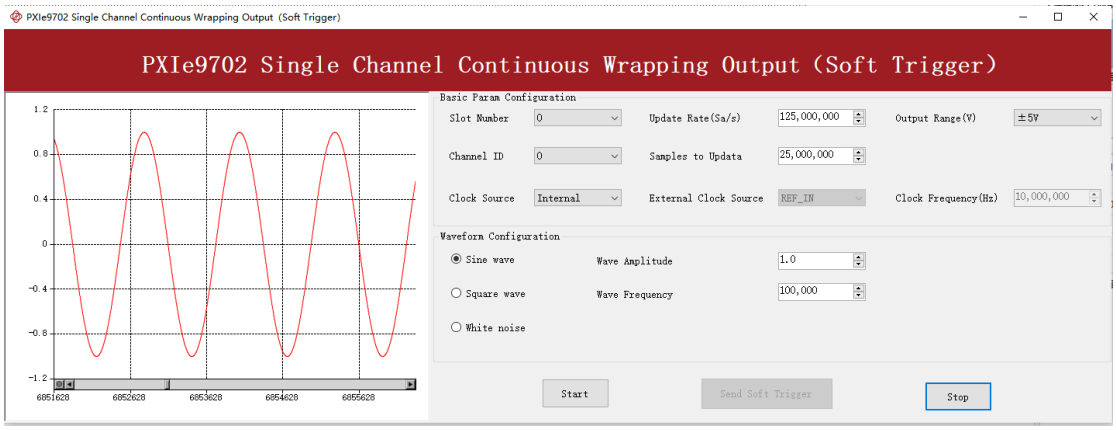

Figure 14 Software Trigger Acquisition

■ And the received signal is shown below.

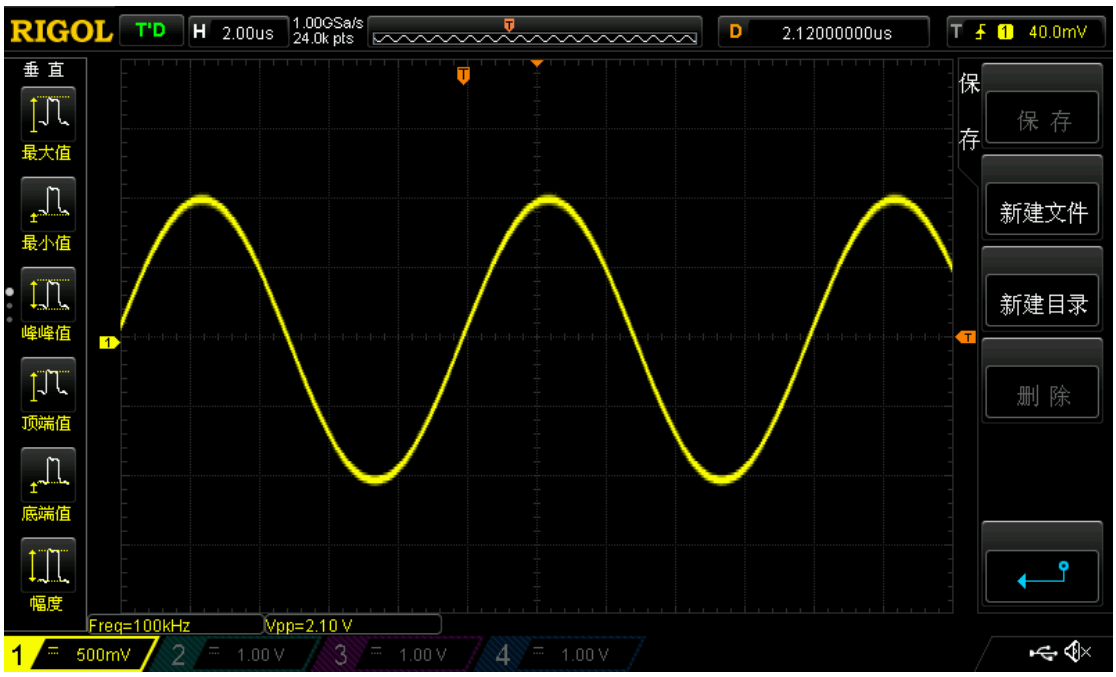

Figure 15 Scope Acquisition AO Signal

- The signal's Freq=100kHz,Vpp=2.08V,which matches the configurations set before.

5.2.3 External Digital Trigger

The module supports different external digital trigger sources from PXI Trigger bus (PXI_TRIG<0..7>), PXI_STAR and connectors of front panel (PFI). The high pulse width of digital trigger signal must be longer then 20 ns for effective trigger. The module will monitor the signal on digital trigger source and wait for the rising edge or falling edge of digital signal which depending on the set trigger condition, then cause the module to output the data as shown in Figure 16

Figure 16 External Digital Trigger

Learn by Example 5.2.3

- Connect the digital trigger source positive terminal to PXIe 9702 TRIG _IN and connect the oscilloscope's CH1 to PXIe-9702's CH0 as shown in Figure 2.
- Set a squarewave signal(4Hz,Vpp=5V).
- Open **Analog Output-->Winform AO Countinuous Wrapping Digtial Trigger**,set the following numbers as shown.

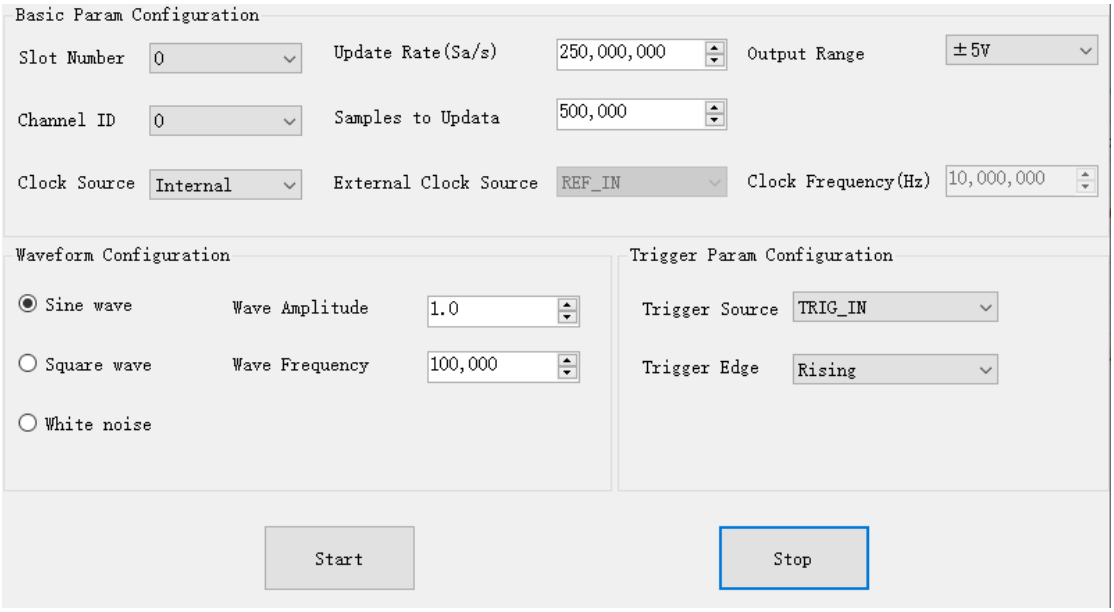

Figure 17 Digital Trigger Paraments

- **Trigger Source** must match the pin on 9702.
- There are four **Trigger Edge:Rising** ,**Falling,High** and **Low.**

- Click **Start** and the result shows below:

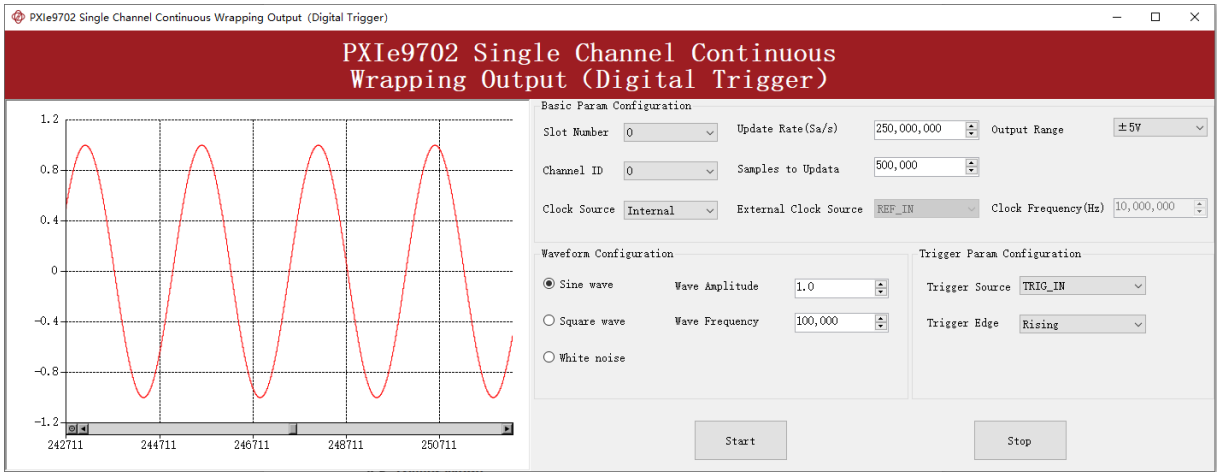

Figure 18 Digital Trigger Acquisition

- Since the squarewave is used for the digital trigger source,when a rising edge of the squarewave occurs,the digital trigger will be activated,and the signal will be generated.

- And the received signal is shown below.

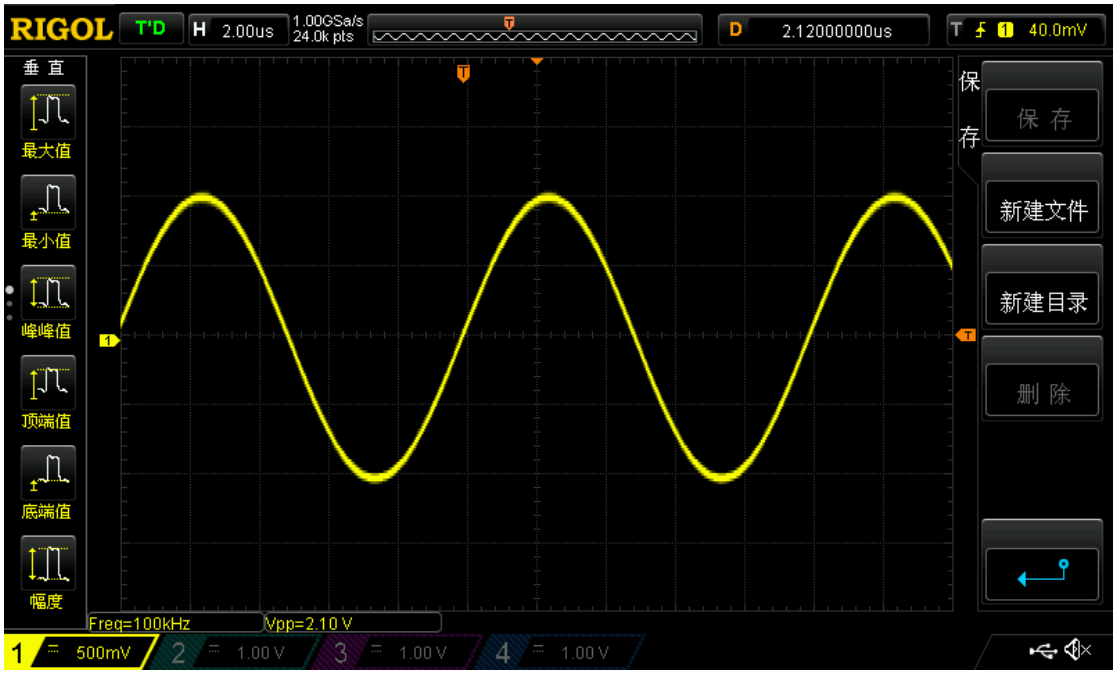

Figure 19 Scope Acquisition AO Signal

- The signal's Freq=100kHz,Vpp=2.08V,which matches the configurations set before.

5.3 Trigger Mode

PXIe-9702 supports one trigger mode: start trigger. Please see the provided software examples for more information.

5.3.1 Start Trigger

In this mode, data output begins immediately after the trigger. This trigger mode is suitable for continuous acquisition and finite acquisition. As shown in Figure 20. Please see the provided software examples for more information.

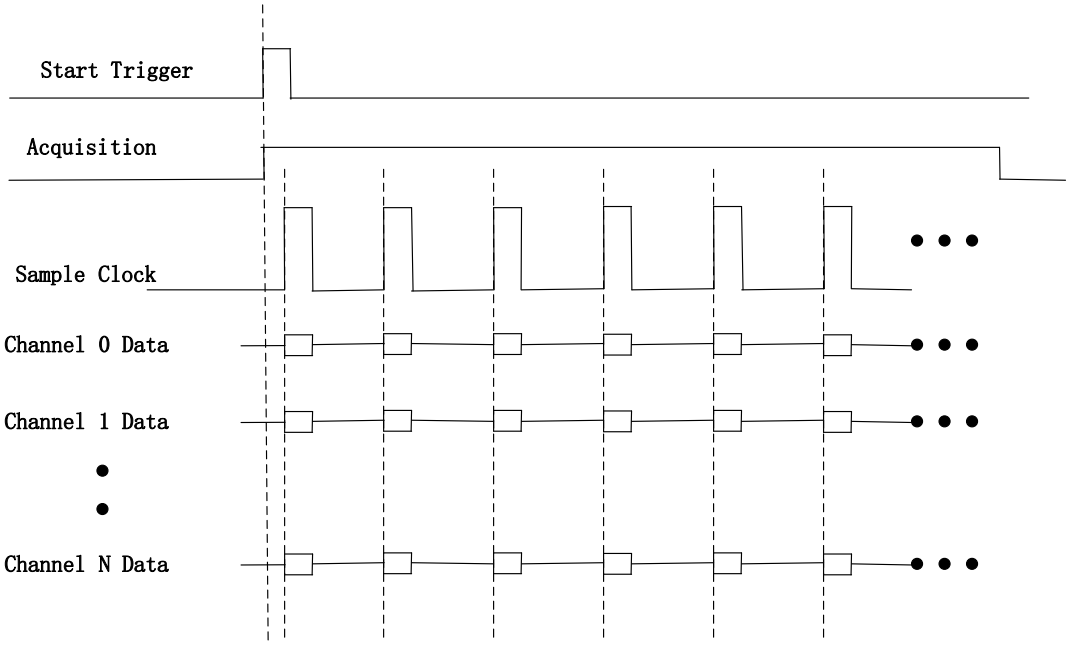

Figure 20 Start Trigger

5.4 AO Operations

The PXIe-9702 AO provides 16-bit simultaneous outputs. The analog output has three modes of operation: finite output, continuous acyclic output, continuous cycle output. Please see the provided software examples for more information.

5.4.1 Finite Output

The finite output requires the user to write a piece of data. After starting the AO, it starts to output the written data until the output is completed.

Learn by Example 5.4.1

- Connect the oscilloscope's CH1 to PXIe-9702's CH0 as shown in Figure 2.
- Open **Analog Output-->Winform AO Finite**,set the following numbers as shown.

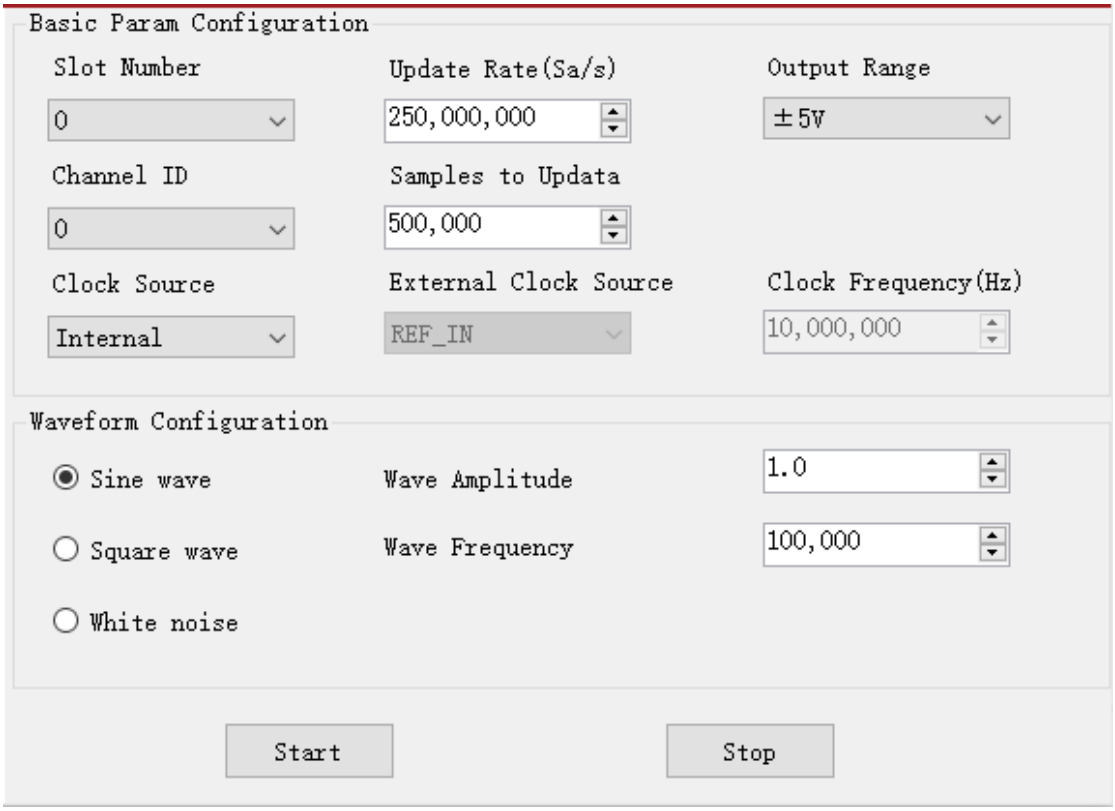

Figure 21 AO Finite Output Paraments

- There are two clock sources in PXIe-9702 *Internal* and *External*:This example uses **Internal** mode set by **Clock Source.**

- Click **Start** to generate a **Sine wave**.The generated signal is shown below.

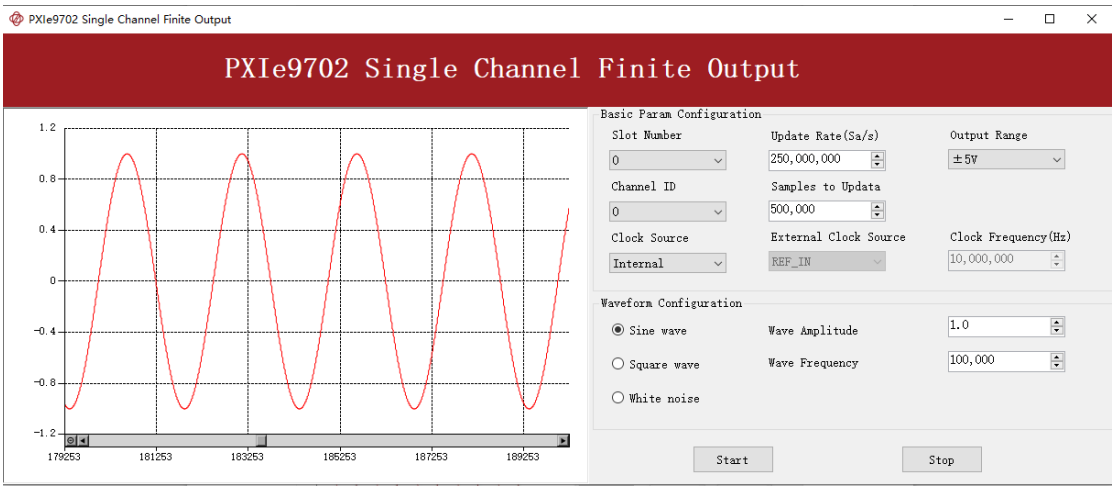

Figure 22 AO Finite Signal

- Change the **Clock Source** to **External**,choose **REF_IN** as **External Clock Source**，and make sure **Clock Frequency** and Signal Generator's frequency are set to the same value.
- Click **Start** to generate a **Sine wave**.The generated signal is shown below.

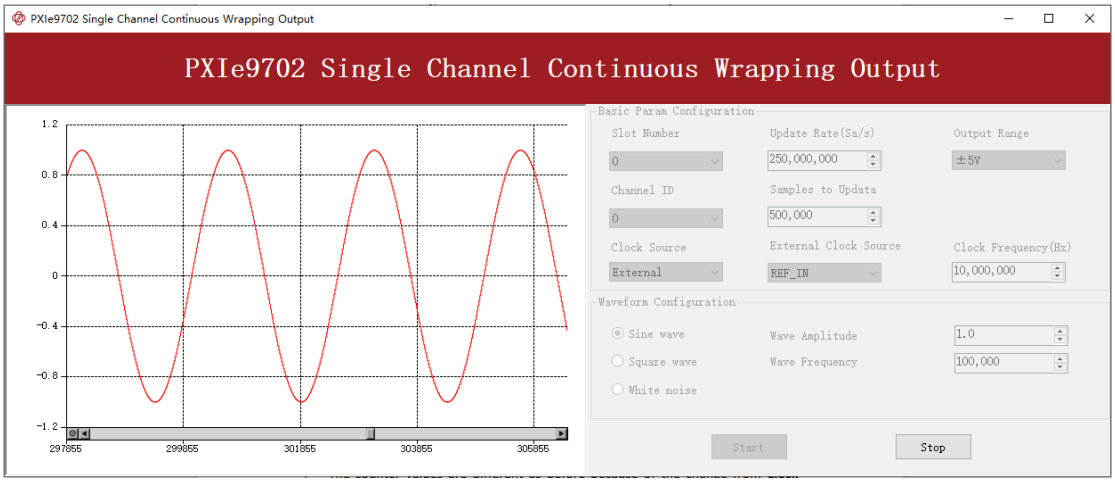

Figure 23 AO Finite Signal (External Clock Source)

- And the received signal is shown below.

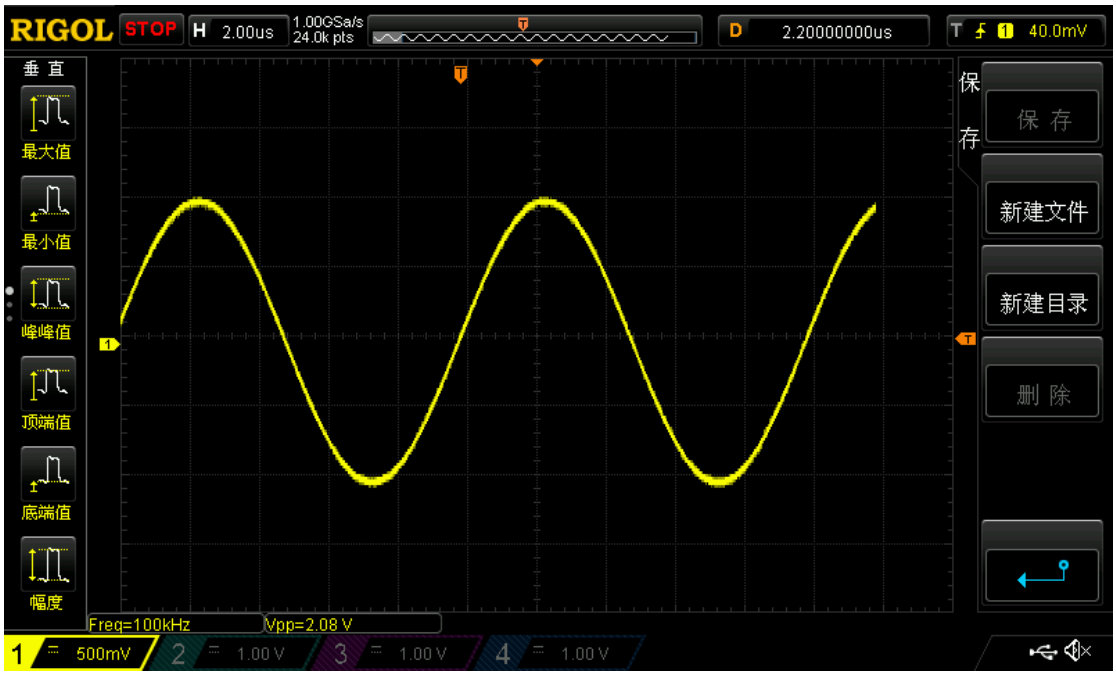

Figure 24 Scope Acquisition AO signal

➢ The analog signal is successfully generated and received by oscilloscope.

➢ The signal's Freq=100kHz,Vpp=2.08V,which matches the configurations set before.

5.4.2 Continuous NoWrappping Output

The continuous acyclic output needs to write a piece of data before starting the AO. After the AO starts, user needs to continuously write new data to ensure the continuous output of the AO.

Learn by Example 5.4.2

- Connect the oscilloscope's CH1 to PXIe-9702's CH0 as shown in Figure 2.
- Open **Analog Output-->Winform AO Continuous NoWrapping**,set the following numbers as shown.

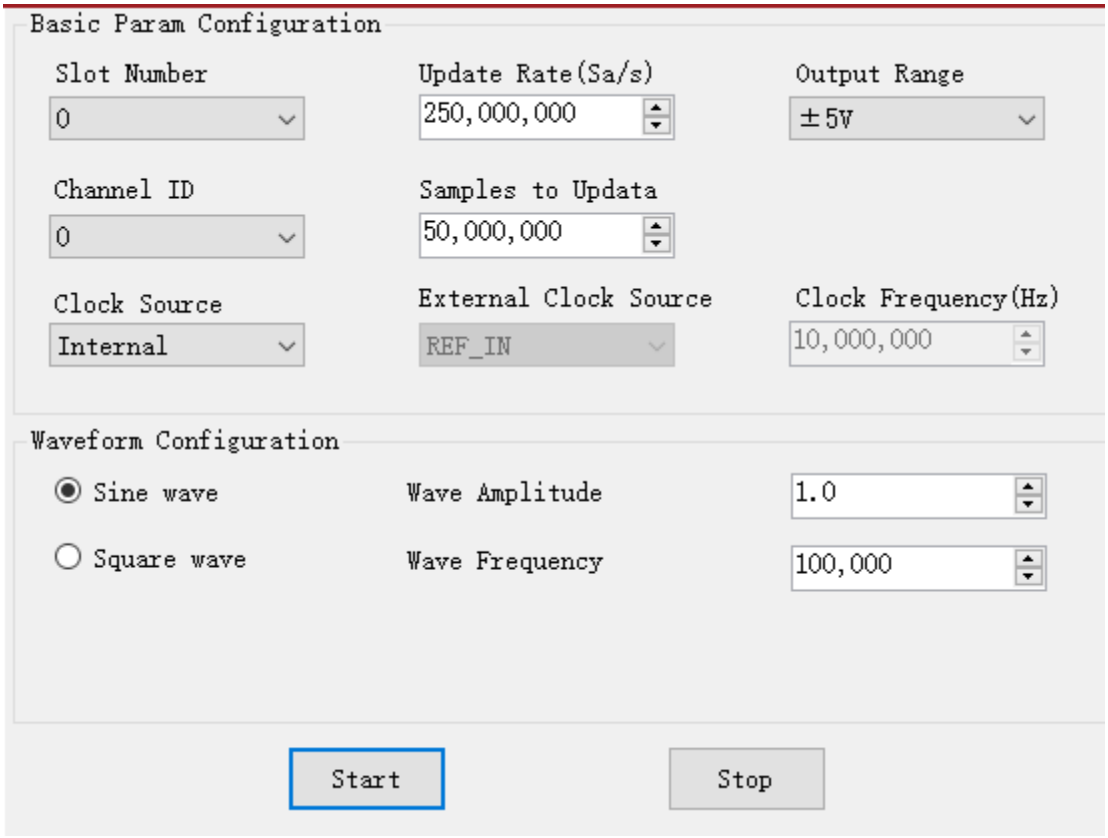

Figure 25 AO Continuous NoWrapping Output Paraments

➢ In no wrapping analog output you can change the paraments of the signal whenever you want in **Waveform Configuration** when generate the wave.You can configuration the paraments after click **Stop**,and then click **Start** to apply the changes.

■ Click **Start** to generate a sinewave first.The result is shown below.

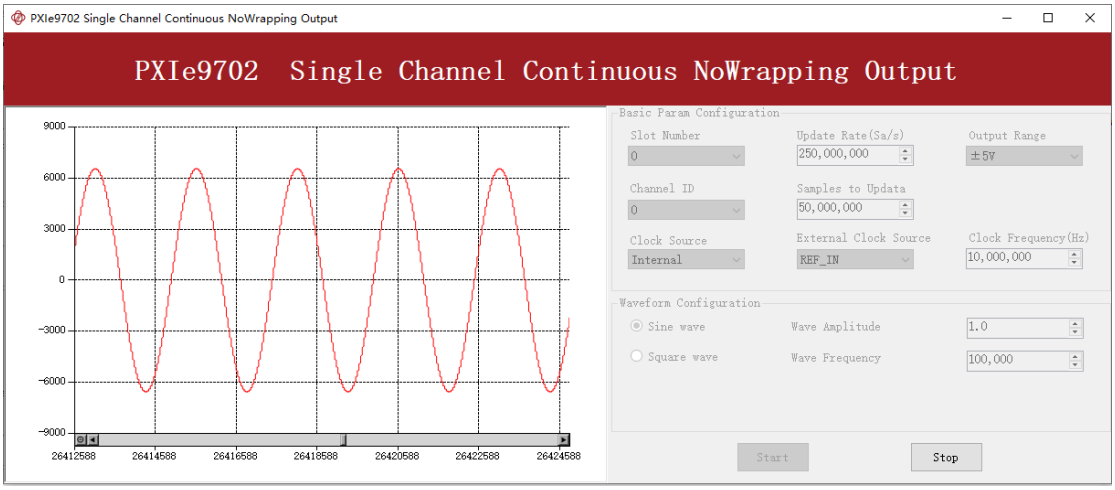

Figure 26 AO Continuous NoWrapping Signal

■ And the received signal is shown below.

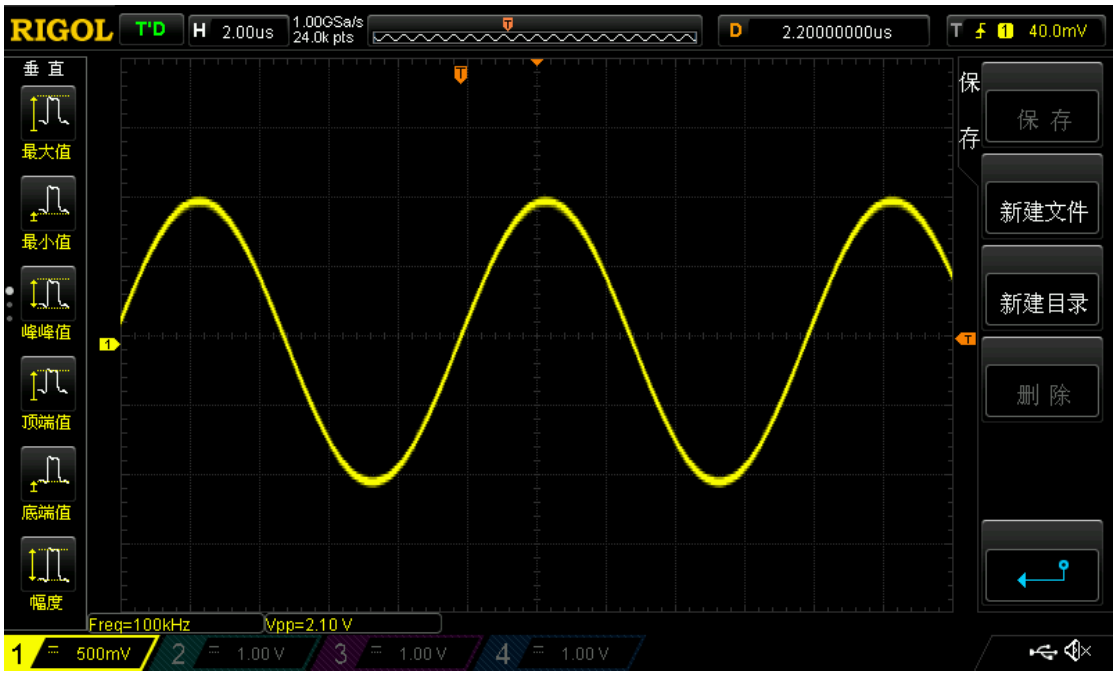

Figure 27 Scope Acquisition AO signal

➢ The signal's Freq=100kHz,Vpp=2.08V,which matches the configurations set before.

■ Now change the WaveType to Square wave.The result is shown below.

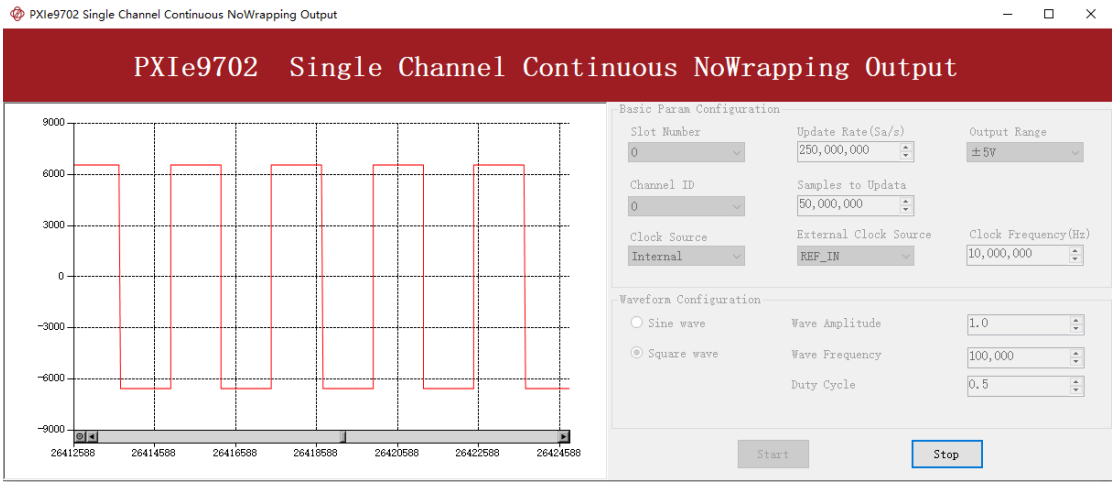

Figure 28 AO Continuous NoWrapping Signal

■ And the received signal is shown below.

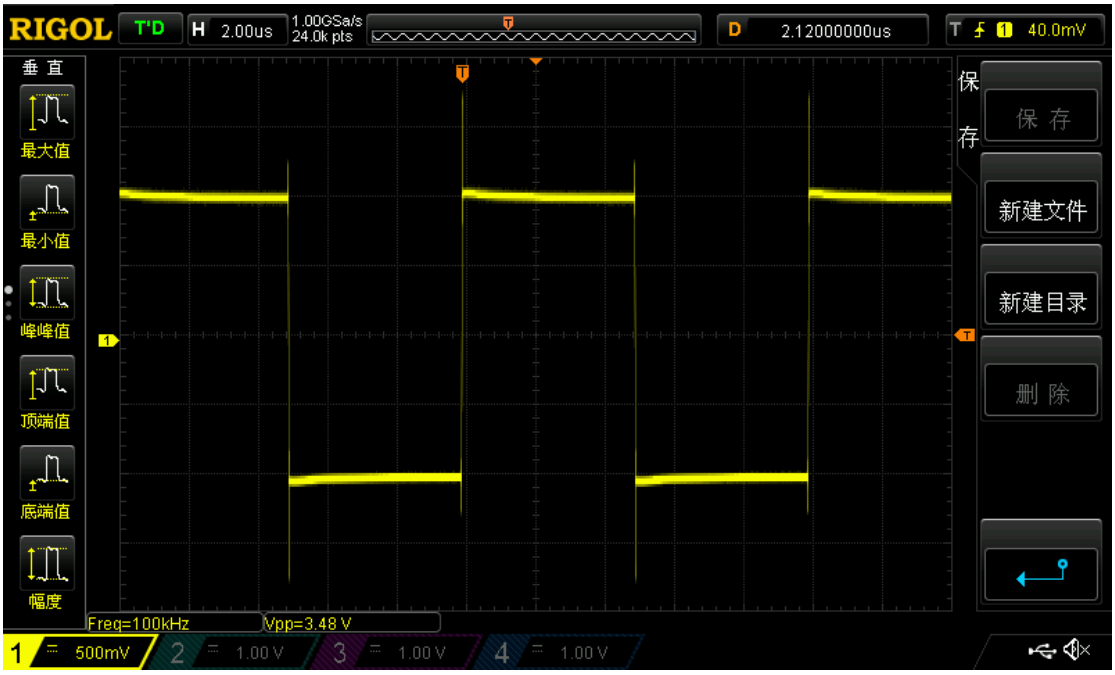

Figure 29 Scope Acquisition AO signal

- The analog signal is successfully generated and received.
- The signal's Freq=100kHz,Vpp=2.08V,which matches the configurations set before.

5.4.3 Continuous Wrapping Output

The continuous loop output first writes a piece of data before starting the AO. After the AO starts, the board will repeatedly output this data until user sends a stop command.

Learn by Example 5.4.3

- Connect the oscilloscope's CH1 to PXIe-9702's CH0 as shown in Figure 2.
- Open **Analog Output-->Winform AO Continuous Wrapping**,set the following numbers as shown.

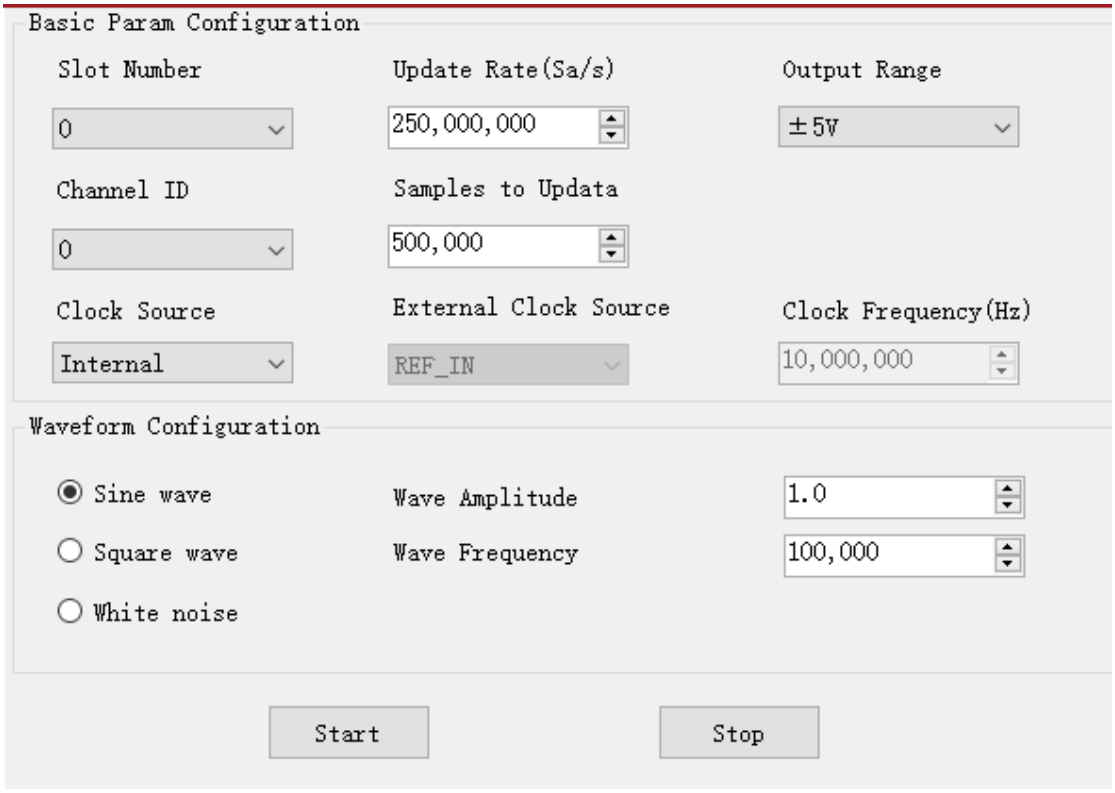

Figure 30 AO Continuous Wrapping Paraments

- Click **Start** to generate the signal.The result is shown below.

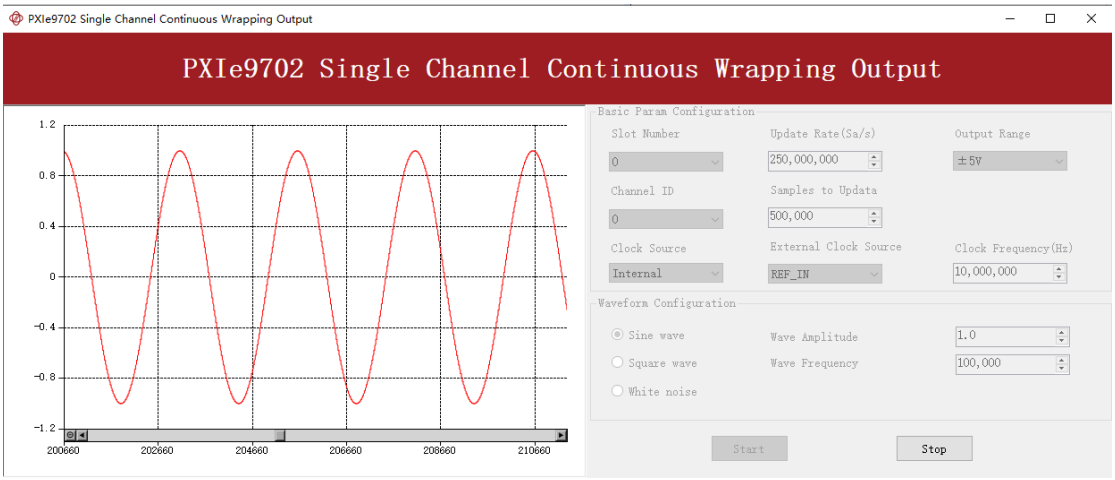

Figure 31 AO Continuous Wrapping Signal

■ And the received signal is shown below.

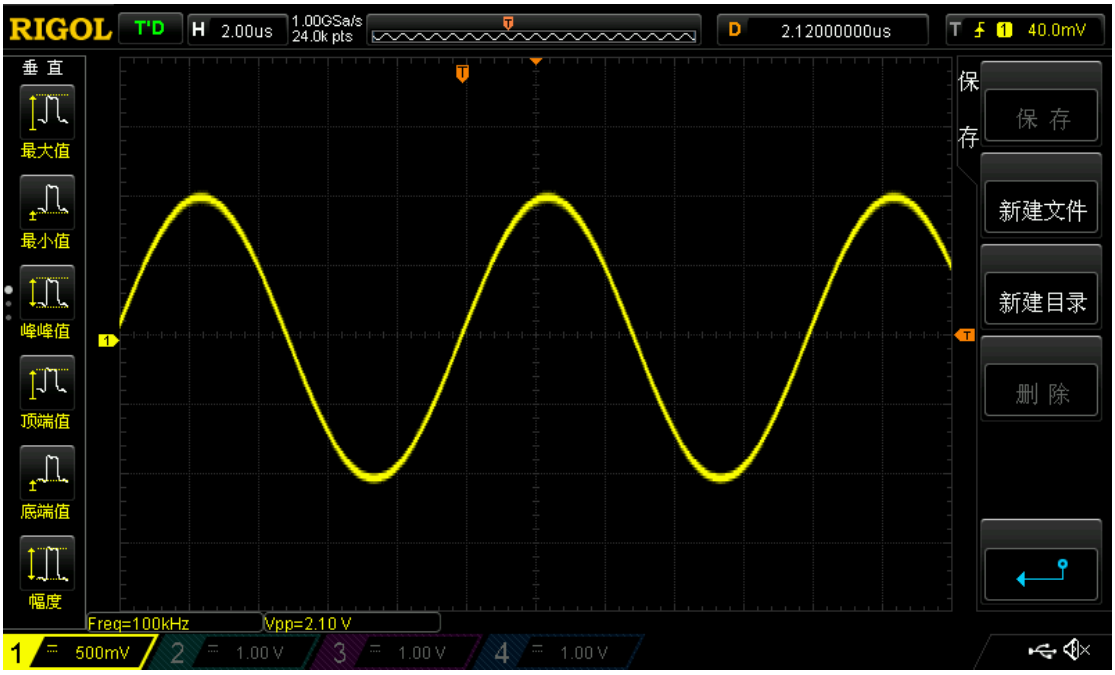

Figure 32 Scope Acquisition AO signal

- The analog signal is successfully generated and received.
- The signal's Freq=100kHz,Vpp=2.08V,which matches the configurations set before.

■ If you want generate two signals,you can connect the oscilloscope's CH1 and CH2 to PXIe-9702's CH0 and CH1 as shown in Figure 3.

- Open **Analog Output-->Winform AO Continuous Wrapping MultiChannel**,set the following numbers as shown.
- Click **Start** to generate two signals,and the received signals is shown below.

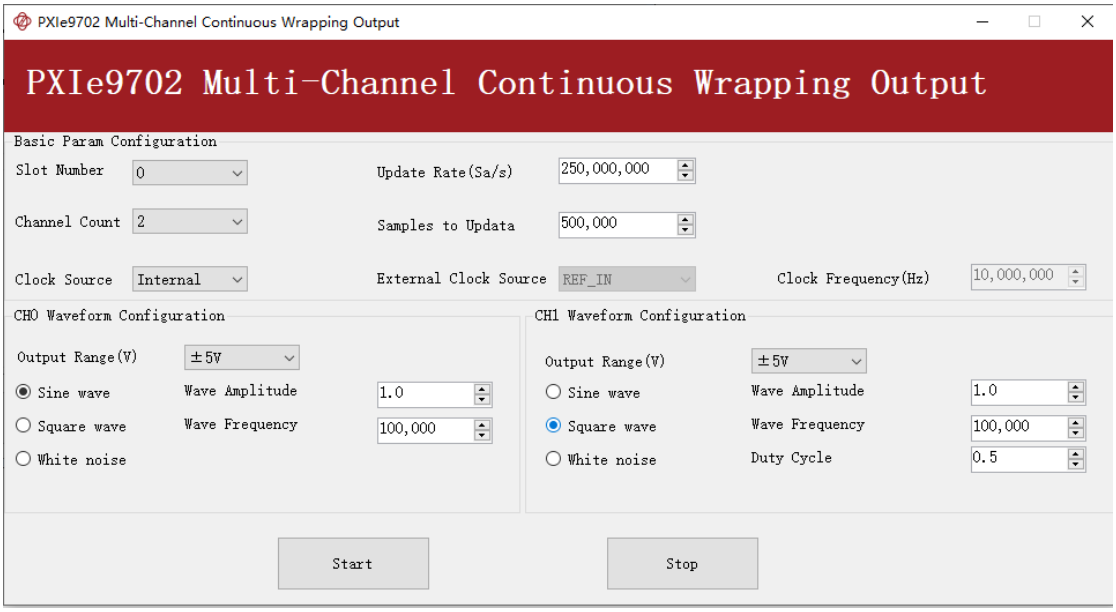

Figure 33 AO Continuous Wrapping MultiChannel Paraments

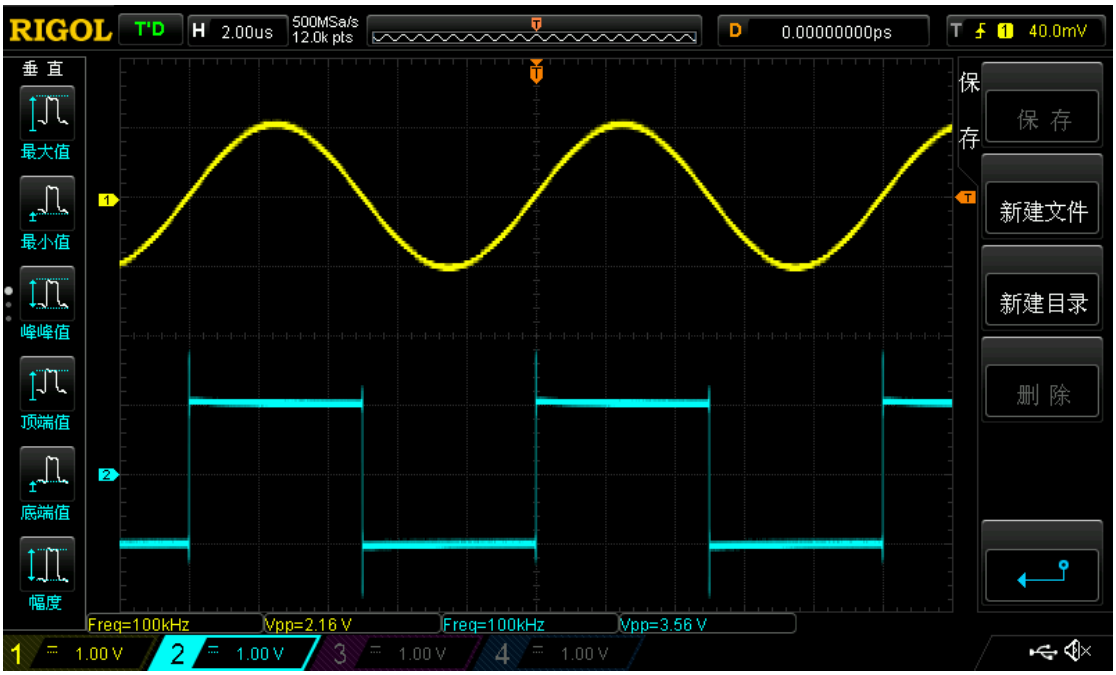

Figure 34 Scope Acquisition AO signal

- The analog signal is successfully generated and received.
- The signal's Freq=100kHz,Vpp=2.08V,the first signal is sinewave,and the second signal is squarewave,which matches the configurations set before.

5.4.4 DDS

DDS (Direct Digital Synthesis) function can be used to generate standard waveform including sine wave/squre wave/triangle wave. Continuous Wrapping Mode may generate breakpoints when updaterate cannot divide signal frequency exactly, while DDS mode will not. Users can configure several parameter for DDS generation including: WaveformType(Sine/Squre/Triangle), Frequency, Amplitude, Offset, DutyCycle(for squre and triangle wave), PhaseOffset, PhaseCompare.

Learn by Example 5.4.4

- Connect the oscilloscope's CH1 and CH2 to PXIe-9702's CH0 and CH1 as shown in Figure 3.
- Open **Analog Output-->Winform AO Standard Waveform generation**,set the following numbers as shown.

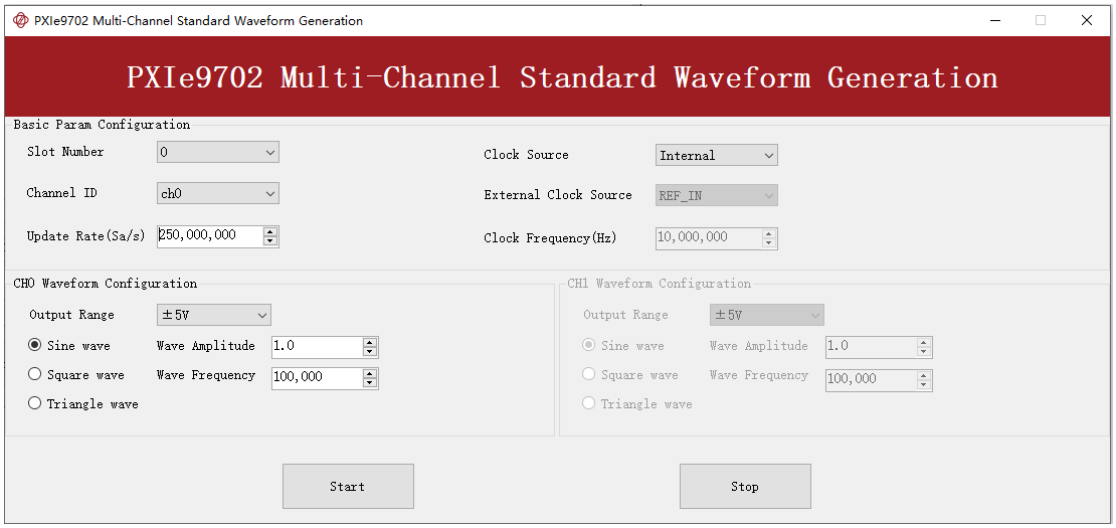

Figure 35 AO Standard Waveform generation Paraments

- Click **Start** to generate the signal.The received signal is shown below.

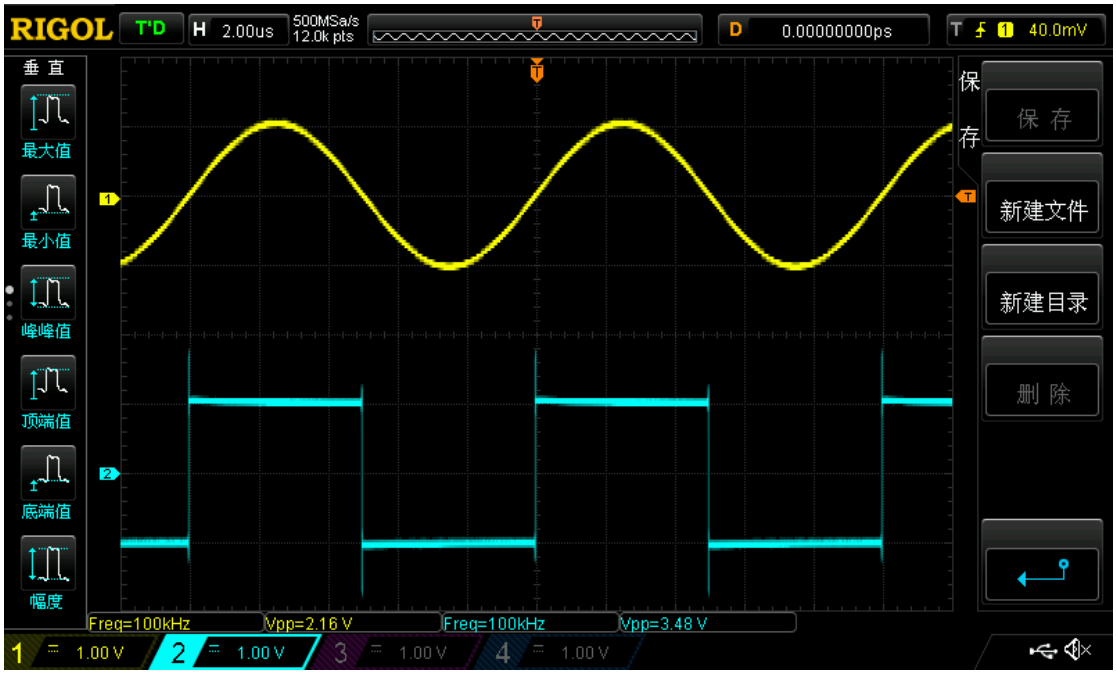

Figure 36 Scope Acquisition AO signal

- The analog signal is successfully generated and received.
- The signal's Freq=100kHz, Vpp=2.08V, the first signal is sinewave, and the second signal is squarewave, which matches the configurations set before.

5.4.5 Output Wave From File

This function can output wave from a .csv file which can be generated by software or yourself.

Learn by Example 5.4.5

- Connect the oscilloscope's CH1 to PXIe-9702's CH0 as shown in Figure 2.
- Open **Analog Output-->Winform AO Output Wave From File**, click **Write File** to generate a .csv file, or you can click **Select** to open a .csv file which is generated by yourself before.

■ Click **Start** to generate a wave from .csv file, the generated signal is shown below.

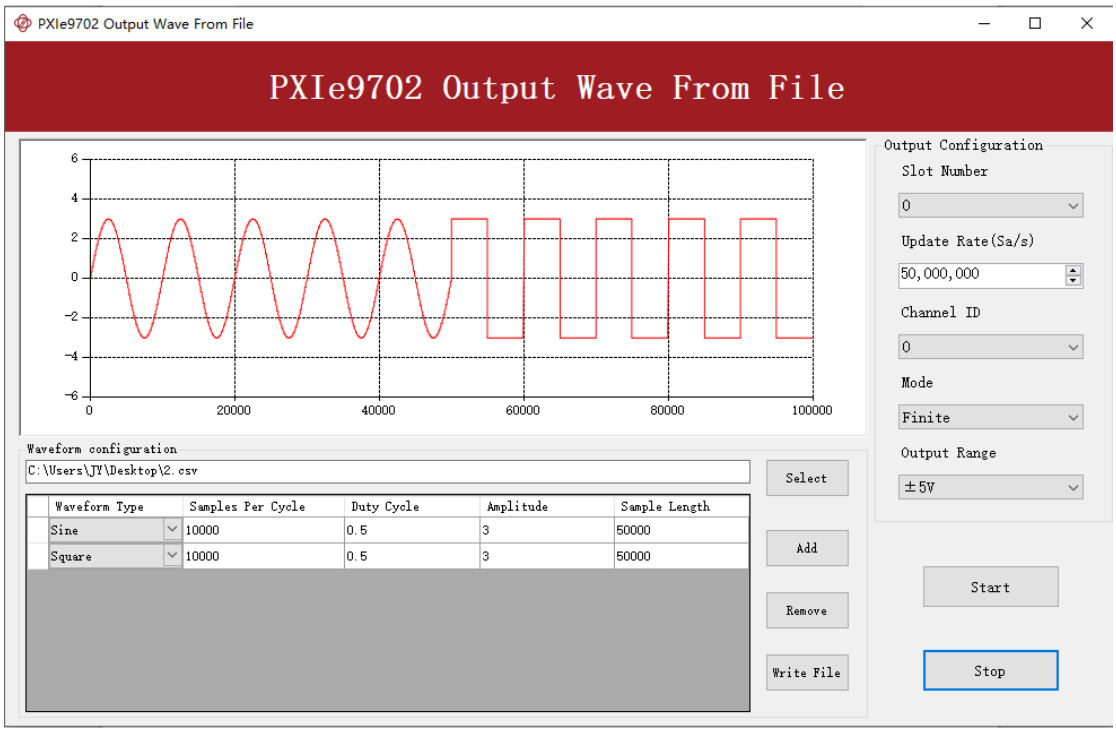

Figure 37 Generated Signal

■ And the received signal is shown below.

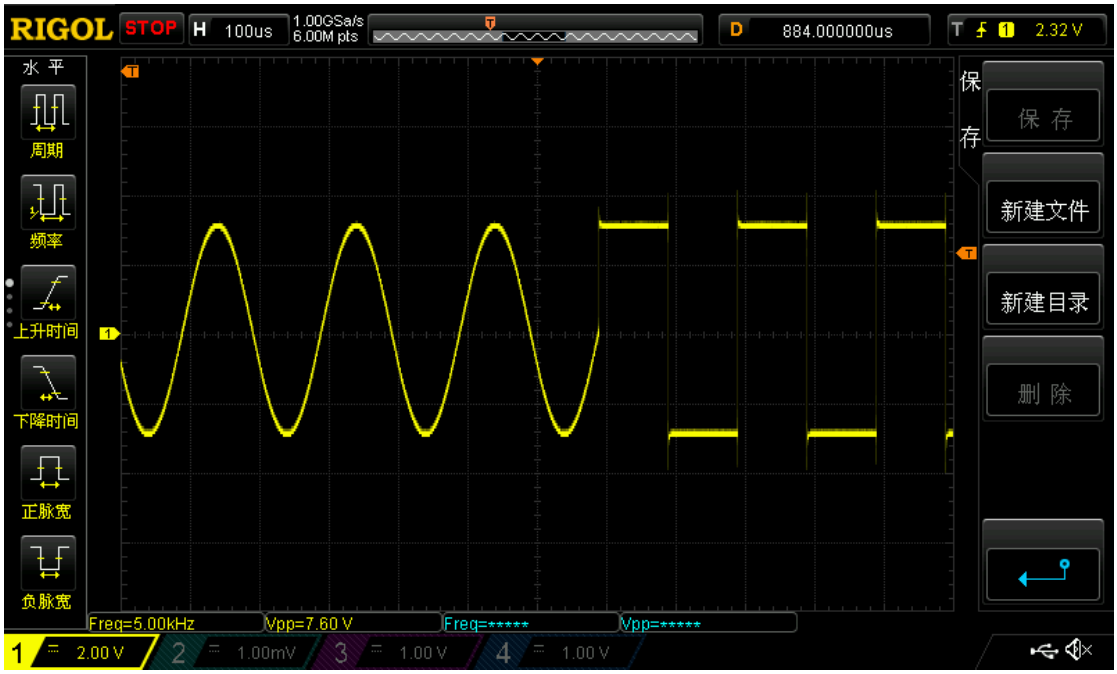

Figure 38 Received Signal

6. Calibration

PXIe-9702 Series boards are precalibrated before the shipment. We recommend you recalibrate PXIe-9702 board periodically to ensure the measurement accuracy. A commonly accepted practice is one year. If for any reason, you need to recalibrate your board, please contact JYTEK.

7. Using PXIe-9702 in Other Software

While JYTEK's default application platform is Visual Studio, the programming language is C#, we recognize there are other platforms that are either becoming very popular or have been widely used in the data acquisition applications. Among them are Python, C++ and LabVIEW. This chapter explains how you can use PXIe-9702 DAQ card using one of this software.

7.1 Python

JYTEK provides and supports a native Python driver for PXIe-9702 boards. There are many different versions of Python. JYTEK has only tested in CPython version 3.5.4. There is no guarantee that JYTEK python drivers will work correctly with other versions of Python.

If you want to be our partner to support different Python platforms, please contact us.

7.2 C++

JYTEK internaly uses our C++drivers to design the C# drivers. We recommend our customers to use C# drivers because C# platform deliver much better efficiency and performance in most situations. We also make our C++ drivers available. However, due to the limit of our resources, we do not actively support C++ drivers. If you want to be our partner to support C++ drivers, please contact us.

7.3 LabVIEW

LabVIEW is a software product from National Instruments. JYTEK provides LabVIEW interface to PXIe-9702 boards. You can down load the LabVIEW dirvers from our website. While JYTEK does not support LabVIEW applications, we may recommend you to a third party who can assist you to interface your LabVIEW with our PXIe-9702 boards. We can also recommend you if you want to convert your LabVIEW applications to C# based applications.

8. About JYTEK

8.1 JYTEK China

Founded in June, 2016, JYTEK China is a leading Chinese test & measurement company, providing complete software and hardware products for the test and measurement industry. The company has evolved from re-branding and reselling PXI(e) and DAQ products to a fully-fledged product company. The company offers complete lines of PXI, DAQ, USB products. More importantly, JYTEK has been promoting open-sourced based ecosystem and offers complete software products. Presently, JYTEK is focused on the Chinese market. Our Shanghai headquarters and production service center have regular stocks to ensure timely supply; we also have R&D centers in Xi'an and Chongqing. We also have highly trained direct technical sales representatives in Shanghai, Beijing, Tianjin, Xi'an, Chengdu, Nanjing, Wuhan, Guangdong, Haerbin, and Changchun. We also have many patners who provide system level support in various cities.

8.2 JYTEK Software Platform

JYTEK has developed a complete software platform, SeeSharp Platform, for the test and measurement applications. We leverage the open sources communities to provide the software tools. Our platform software is also open sourced and is free, thus lowering the cost of tests for our customers. We are the only domestic vendor to offer complete commercial software and hardware tools.

8.3 JYTEK Warranty and Support Services

With our complete software and hardware products, JYTEK is able to provide technical and sales services to wide range of applications and customers. In most cases, our products are backed by a 2-year warranty. For technical consultation, pre-sale and after-sales support, please contact JYTEK of your country.

9. **Statement**

The hardware and software products described in this manual are provided by JYTEK China, or JYTEK in short.

This manual provides the product review, quick start, some driver interface explaination for JYTEK PXIe-9702 Series family of multi-function data acquisition boards. The manual is copyrighted by JYTEK.

No warranty is given as to any implied warranties, express or implied, including any purpose or non-infringement of intellectual property rights, unless such disclaimer is legally invalid. JYTEK is not responsible for any incidental or consequential damages related to performance or use of this manual. The information contained in this manual is subject to change without notice.

While we try to keep this manual up to date, there are factors beyond our control that may affect the accuracy of the manual. Please check the latest manual and product information from our website.

Shanghai JYTEK Co., Ltd.

Address: Building 3, No. 300 Fangchun Road, Pudong New District, Shanghai.

Post Code: 201203

Tel: 021-5047 5899

Website: www.jytek.com